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ORIGINALLY FILED

IP 2123

PTO/SB/21 (08-00)

Approved for use through 10/31/2002. OMB 0651-0031  
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

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## TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Application No.	09/148,392
Filing Date	September 4, 1998
First Named Inventor	Franklin M. Baez
Group Art Unit	2123
Examiner Name	W. Thomson
Total Number of Pages in This Submission	24
Attorney Docket Number	42390P5512

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### ENCLOSURES (check all that apply)

<input checked="" type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Assignment Papers (for an Application)	<input type="checkbox"/> After Allowance Communication to Group
<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
<input type="checkbox"/> Amendment / Response	<input type="checkbox"/> Licensing-related Papers	<input type="checkbox"/> Appeal Communication to Group (Appeal Notice, Brief, Reply Brief)
<input type="checkbox"/> After Final	<input type="checkbox"/> Petition	<input type="checkbox"/> Proprietary Information
<input type="checkbox"/> Affidavits/declaration(s)	<input type="checkbox"/> Petition to Convert a Provisional Application	<input type="checkbox"/> Status Letter
<input type="checkbox"/> Extension of Time Request	<input type="checkbox"/> Power of Attorney, Revocation, Change of Correspondence Address	<input checked="" type="checkbox"/> Other Enclosure(s) (please identify below):
<input type="checkbox"/> Express Abandonment Request	<input type="checkbox"/> Terminal Disclaimer	1. Request for Withdrawal of Abandonment, 2. Copy of postcard, Amendment and Response to Office Action mailed
<input type="checkbox"/> Information Disclosure Statement	<input type="checkbox"/> Request for Refund	
<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> CD, Number of CD(s)	
<input type="checkbox"/> Response to Missing Parts/ Incomplete Application		
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53		
Remarks		

### SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Thinh V. Nguyen, Reg. No. 42,034  BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	January 29, 2002

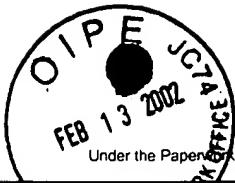
### CERTIFICATE OF MAILING/TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail with sufficient postage in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on:

January 29, 2002

Typed or printed name	Barbara Hayashi
Signature	
Date	January 29, 2002

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# FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

 Applicant claims small entity status. See 37 CFR 1.27.

TOTAL AMOUNT OF PAYMENT (\$)

## Complete if Known

Application Number	09/148,392
Filing Date	September 4, 1998
First Named Inventor	Franklin M. Baez
Examiner Name	W. Thomson
Group/Art Unit	2123
Attorney Docket No.	42390P5512

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## METHOD OF PAYMENT (check one)

Check     Credit card     Money Order     Other     None

Deposit Account

Deposit Account Number **02-2666**Deposit Account Name **Blakely, Sokoloff, Taylor & Zafman LLP**

The Commissioner is authorized to: (check all that apply)

Charge fee(s) indicated below     Credit any overpayments

Charge any additional fee(s) during the pendency of the application

Charge fee(s) indicated below, except for the filing fee to the above-identified deposit account

## FEE CALCULATION

## 1. BASIC FILING FEE

Large Entity	Small Entity	Fee Description	Fee Paid
Fee Code	Fee (\$)	Fee Code	Fee (\$)
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107	510	207	255 Plant filing fee
108	740	208	370 Reissue filing fee
114	160	214	80 Provisional filing fee
SUBTOTAL (1)		(\$)	

## 2. EXTRA CLAIM FEES

Total Claims	Independent Claims	Extra Claims	Fee from below	Fee Paid
28	4	** = <input type="text"/>	X <input type="text"/>	= <input type="text"/>

Large Entity	Small Entity	Fee Description
Fee Code	Fee (\$)	Fee Code
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102	84	202 42 Independent claims in excess of 3
104	280	204 140 Multiple Dependent claim, if not paid
109	84	209 42 **Reissue independent claims over original patent
110	18	210 9 **Reissue claims in excess of 20 and over original patent
SUBTOTAL (2)		(\$)

\*\*or number previously paid, if greater. For Reissues, see below

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126	180	126 180 Submission of Information Disclosure Stmt	
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149	740	249 370 For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279 370 Request for Continued Examination (RCE)	
169	900	169 900 Request for expedited examination of a design application	
Other fee (specify)			

\*Reduced by Basic Filing Fee Paid

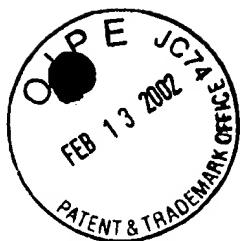
SUBTOTAL (3) (\$)

## SUBMITTED BY

Name (Print/Type)	Thinh V. Nguyen	Registration No. (Attorney/Agent)	42,034	Telephone	(714) 557-3800
Signature				Date	01/29/02

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Our Docket No.: 042390.P5512

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Franklin M. Baez

Application No.: 09/148,392

Filed: September 4, 1998

For: DESIGN OPTIMIZATION OF  
CIRCUITS BY SELECTING DESIGN  
POINTS ON PARAMETER  
FUNCTIONS TO IMPROVE  
OPTIMIZING PARAMETERS OF  
CIRCUITS WITHIN DESIGN  
CONSTRAINTS

Examiner: William D. Thomson

Art Group: 2123

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**REQUEST FOR WITHDRAWAL OF ABANDONMENT**

Assistant Commissioner for Patents  
Washington, DC 20231

Dear Sir:

In response to the Notice of Abandonment mailed January 14, 2002, Applicant respectfully requests the abandonment be withdrawn for the following reasons:

1. Applicant filed a response to the Office Action dated April 24, 2001, on October 24, 2001, with a three-month extension.
2. The Examiner telephoned the Applicant on November 6, 2001 to advise that he was going to issue a Notice of Abandonment. The Applicant advised the Examiner at that time that a response was filed on October 24, 2001 with a three-month extension. The Examiner replied that he would call the Applicant and request a faxed copy of the response if he did not receive it soon.

Applicant hereby encloses copies of the following:

1. A copy of the Amendment and Response to the Office Action showing a Certificate of Mailing executed on October 24, 2001; and
2. A copy of the postcard confirming the Patent and Trademark Office's receipt of the Amendment and Response to the Office Action.

Please proceed with further examination of this application on the basis of the attached copy of the papers originally filed.

Acknowledgement of the active status of this application is respectfully requested.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

  
\_\_\_\_\_  
THINH V. NGUYEN

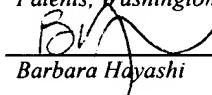
Reg. No. 42,034

Dated: January 29, 2002

12400 Wilshire Boulevard, Seventh Floor  
Los Angeles, California 90025  
(714) 557-3800

**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: January 29, 2002.

  
\_\_\_\_\_  
Barbara Hayashi



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COSTA MESA

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JAN 18 2002

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN  
LOS ANGELES

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FEB 22 2002  
Technology Center 2100

Application No.: 09/148,392 Filing Date: 09/04/98 BSTZ Docket #: 42390P5512 Atty/Sec: TVN/bh  
Date Mailed: 10/24/2001 Docket Due Date(s): 10/24/2001 Client: Intel Corporation  
Title Design Optimization of Circuits by Selecting Design Points on Parameter Functions to Improve Optimizing Parameters of Circuits Within Design Constraints

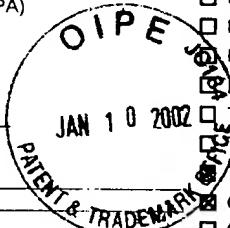
Inventor(s) Baez

The following has been received in the U.S. Patent & Trademark Office on the date stamped hereon:

Amendment: (13 pgs)  
 Appeal Brief & two copies ( pgs)  
 Application:  
( pages w/ cover & abstract)  
 Assignment & Cover Sheet ( pgs)  
 Certificate of Mailing  
 Continued Prosecution Application (CPA)  
 Declaration & POA ( pgs)  
 Drawings: sheets, figures  
 Express Mail No: \_\_\_\_\_  
 Extension of Time: three (3) months  
 Fee Transmittal (original & copy)  
 Other \_\_\_\_\_

Information Disclosure Statement & PTO/SB/08 ( pgs)  
 Issue Fee Transmittal (original & copy)  
 Notice of Appeal  
 Petition for: \_\_\_\_\_  
 Request for Continued Examination (RCE)  
 Reply Brief ( pgs)  
 Request and Certification Under 35 U.S.C. 122(b)(2)(B)(i)  
 Request to Rescind Previous Nonpublication Request  
 Response to Notice of Missing Parts & Formalities Letter  
 Terminal Disclaimer  
 Transmittal of Formal Drawings  
 Transmittal Letter  
 Check No. 12626 in the Amount of \$1,022.00  
 Check No. in the Amount of \_\_\_\_\_

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JAN 18 2002

STATUS DB-LA



PTO/SB/21 (12/97)

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Patent and Trademark Office, U.S. DEPARTMENT OF COMMERCE

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**TRANSMITTAL FORM**

(to be used for all correspondence after initial filing)

		Application No.	09/148,392
		Filing Date	September 4, 1998
		First Named Inventor	Franklin M. Baez
		Group Art Unit	2123
		Examiner Name	W. Thomson
Total Number of Pages in This Submission	17	Attorney Docket Number	42390P5512

**ENCLOSURES (check all that apply)**

<input checked="" type="checkbox"/> Fee Transmittal Form	<input type="checkbox"/> Assignment Papers <i>(for an Application)</i>	<input type="checkbox"/> After Allowance Communication to Group
<input type="checkbox"/> Fee Attached	<input type="checkbox"/> Drawing(s)	<input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences
<input checked="" type="checkbox"/> Amendment / Response	<input type="checkbox"/> Licensing-related Papers	<input type="checkbox"/> Appeal Communication to Group <i>(Appeal Notice, Brief, Reply Brief)</i>
<input type="checkbox"/> After Final	<input type="checkbox"/> Petition Routing Slip (PTO/SB/69) and Accompanying Petition	<input type="checkbox"/> Proprietary Information
<input type="checkbox"/> Affidavits/declaration(s)	<input type="checkbox"/> To Convert a Provisional Application	<input type="checkbox"/> Status Letter
<input checked="" type="checkbox"/> Extension of Time Request	<input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address	<input type="checkbox"/> Additional Enclosure(s) <i>(please identify below):</i>
<input type="checkbox"/> Express Abandonment Request	<input type="checkbox"/> Terminal Disclaimer	
<input type="checkbox"/> Information Disclosure Statement	<input type="checkbox"/> Small Entity Statement	
<input type="checkbox"/> Certified Copy of Priority Document(s)	<input type="checkbox"/> Request for Refund	
<input type="checkbox"/> Response to Missing Parts/ Incomplete Application		
<input type="checkbox"/> Response to Missing Parts under 37 CFR 1.52 or 1.53		
	Remarks	

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**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

Firm or Individual name	Thinh V. Nguyen, Reg. No. 42,034  BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Signature	
Date	October 24, 2001

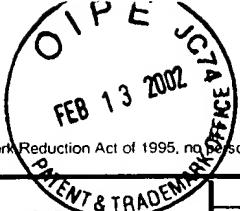
**CERTIFICATE OF MAILING/TRANSMISSION**

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class mail with sufficient postage in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on:

October 24, 2001

Typed or printed name	Barbara Hayashi		
Signature		Date	October 24, 2001

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# FEE TRANSMITTAL for FY 2000

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT (\$ 1,022.00)

## Complete if Known

Application Number	09/148,392
Filing Date	September 4, 1998
First Named Inventor	Franklin M. Baez
Examiner Name	W. Thomson
Group/Art Unit	2123
Attorney Docket No.	42390P55T2

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## METHOD OF PAYMENT (check one)

1.  The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:

Deposit Account Number **02-2666**Deposit Account Name **Blakely, Sokoloff, Taylor & Zafman LLP**

Charge Any Additional Fee(s) Required  
Under 37 CFR §§ 1.16, 1.17, 1.18 and 1.20.

Applicant claims small entity status.  
See 37 CFR 1.27.

2.  Payment Enclosed:

Check  Credit card  Money Order  Other

## FEE CALCULATION

## 1. BASIC FILING FEE

## Large Entity Small Entity

Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) (\$)

## 2. EXTRA CLAIM FEES

Total Claims	Independent Claims	Extra Claims	Fee from below	
28	4	27**	1 X 18.00 = \$18.00	
		3**	1 X 84.00 = \$84.00	

Multiple Dependent

## Large Entity Small Entity

Fee Code	Fee (\$)	Fee Code	Fee (\$)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple Dependent claim, if not paid
109	84	209	42	**Reissue independent claims over original patent
110	18	210	9	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$ 102.00)

\*\*or number previously paid, if greater. For Reissues, see below

## 3. ADDITIONAL FEE

Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Description
105	130	205	65 Surcharge - late filing fee or oath
127	50	227	25 Surcharge - late provisional filing fee or cover sheet.
139	130	139	130 Non-English specification
147	2,520	147	2,520 For filing a request for <i>ex parte</i> reexamination
112	920*	112	920*Requesting publication of SIR prior to Examiner action
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169	900	169	900 Request for expedited examination of a design application

Other fee (specify)

Other fee (specify)

\*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$ 920.00)

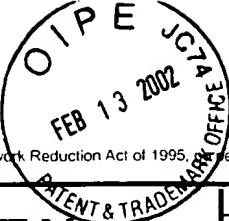
## SUBMITTED BY

## Complete (if applicable)

Name (Print/Type)	Thinh V. Nguyen	Registration No. (Attorney/Agent)	42,034	Telephone	(714) 557-3800
Signature				Date	10/24/01

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Other fee (specify)							
Other fee (specify)							

\*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) (\$ 920.00)

## SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Thinh V. Nguyen	Registration No. (Attorney/Agent)	42,034	Telephone	(714) 557-3800
Signature	<i>Thinh V. Nguyen</i>			Date	10/24/01

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Docket No.: 42390P5512

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

FRANKLIN M. BAEZ

Application No.: 09/148,392

Filed: September 4, 1998

For: **Design Optimization of Circuits by Selecting  
Design Points on Parameter Functions to Improve  
Optimizing Parameters of Circuits Within Design  
Constraints**

Art Group: 2123

Examiner: W. Thomson

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**FEB 22 2002**

**Technology Center 2100**

**PETITION FOR EXTENSION OF TIME PURSUANT TO 37 C.F.R. § 1.136(a)**

Assistant Commissioner for Patents  
Washington, D.C. 20231

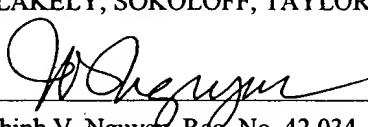
Sir:

In accordance with 37 C.F.R. § 1.136(a), Applicant for the above-identified application respectfully Petitions the Commissioner for a three (3) months month extension of time, extending the period for response to October 24, 2001, from the Office Action dated April 24, 2001. The petition filing fee of 920 and the Response to Office Action are attached.

If it should be determined that a longer extension of time is required to prevent this application from being abandoned, please charge any additional fees to Deposit Account No. 02-2666. A copy of the Fee Transmittal is enclosed for deposit account charging purposes.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

  
Thinh V. Nguyen, Reg. No. 42,034

Date: October 24, 2001

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Barbara Hayashi

10-24-01

Date



*Cop 2/11*

Docket No.: 042390.P5512

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

**Franklin M. Baez**

Application No.: 09/148,392

Filed: September 4, 1998

For: DESIGN OPTIMIZATION OF  
CIRCUITS BY SELECTING DESIGN  
POINTS ON PARAMETER  
FUNCTIONS TO IMPROVE  
OPTIMIZING PARAMETERS OF  
CIRCUITS WITHIN DESIGN  
CONSTRAINTS (Amended)

Examiner: William Thomas

Art Group: 2123

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*Technology Center 2100*

AMENDMENT AND RESPONSE TO THE OFFICE ACTION

BOX NON-FEE AMENDMENT  
Assistant Commissioner for Patents  
Washington, DC 20231-9998

Sir:

In response to the outstanding Office Action, mailed April 24, 2001, please amend the above-identified Application as follows:

**IN THE TITLE**

Please delete the Title of the Application and insert the following in lieu thereof:

--DESIGN OPTIMIZATION OF CIRCUITS BY SELECTING DESIGN POINTS ON  
PARAMETER FUNCTIONS TO IMPROVE OPTIMIZING PARAMETERS OF CIRCUITS  
WITHIN DESIGN CONSTRAINTS--.

## IN THE ABSTRACT

Please delete the Abstract and insert the following in lieu thereof:

--One embodiment of the present invention is a method and machine readable medium for determining optimal values of design parameters of a subsystem to meet design constraints. The subsystem includes a number of circuits. A parameter function is created for the corresponding circuits. The parameter function represents a relationship among design parameters of the subsystem. The design parameters include constraint and optimizing sets. Initial design points for the parameter functions having a first sum of the constraint sets and a second sum of the optimizing sets are selected to such that the first sum satisfies the design constraints. New design points for the parameter functions are selected such that the second sum is improved while the first sum is within the design constraints.--

## IN THE CLAIMS

Following is a complete set of claims as amended with this response, which includes new claims 28 and 29, and amendments to claims 1, 3, 11, 13, 22, and 24.

1

### CLEAN CLAIMS

- 1        1.        (THREE TIMES AMENDED) A method comprising:
  - 2              (a) creating parameter functions for a plurality of circuits in a subsystem, the subsystem  
3              having design constraints, each one of the parameter functions corresponding to each one of the  
4              circuits, the parameter functions representing a relationship among [the] design parameters of the  
5              subsystem, the design parameters including constraint and optimizing sets;
  - 6              (b) selecting initial design points on the parameter functions having a first sum of the  
7              constraint set and a second sum of the optimizing set such that the first sum satisfies the design  
8              constraints; and
  - 9              (c) selecting new design points on the parameter functions such that the second sum is  
10          improved within the design constraints.
- 1        2.        The method of claim 1 wherein the creating the parameter functions comprises:
  - 2              (a1)      configuring each circuit of the plurality of circuits; and

3                   (a2) generating values of design parameters for each circuit according to the  
4 configured circuit, the values providing the parameter functions.

1                 3.     (AMENDED) The method of claim 2 wherein the constraint set includes  
2 constraint parameters having values selectable to meet the design constraints and the optimizing  
3 set includes optimizing parameters having values to be optimized.

1                 4.     (AMENDED) The method of claim 3 wherein selecting the new design points  
2 comprises:

3                 (c1) selecting values of the constraint parameters to meet the design constraints;  
4                 (c2) determining values of the optimizing parameters corresponding to the selected  
5 values of the constraint parameters based on the parameter functions; and  
6                 (c3) iterating c(1) and (c2) until values of the optimizing parameters are within a  
7 predetermined optimal range.

1                 5.     The method of claim 3 wherein the constraint parameters include a delay  
2 parameter and the optimizing parameters include a power parameter.

1                 6.     The method of claim 5 wherein the design constraints include a delay constraint.

1                 7.     The method of claim 6 wherein (a1) comprises:  
2                   sizing components in each circuit.

1                 8.     The method of claim 6 wherein (a1) comprises:  
2                   selecting a design technology for each circuit, the design technology being one of static  
3 and dynamic technologies.

1                 9.     The method of claim 7 wherein (a2) comprises:  
2                 (a21) generating a circuit netlist representing the configured circuit;  
3                 (a22) generating a timing file based on the circuit netlist using a circuit critical path;  
4                 (a23) determining power of the configured circuit based on the circuit netlist;  
5                 (a24) calculating timing values by using a timing simulator; and  
6                 (a25) calculating power values by using a power estimator.

1           10. The method of claim 9 wherein [optimizing] selecting the new design points  
2 comprises:

3           (c1) selecting values of the delay parameter within the delay constraint;

4           (c2) determining values of the power parameter corresponding to the selected values  
5 of the delay parameter based on the parameter function; and

6           (c3) iterating (c1) and (c2) until values of the power parameter are within a  
7 predetermined optimal range.

1           11. (TWICE AMENDED) A machine readable medium having embodied thereon a  
2 computer program for processing by a machine, the computer program comprising:

3           (a) a first code segment to create parameter functions for a plurality of circuits in a  
4 subsystem, the subsystem having design constraints, each one of the parameter functions  
5 corresponding to each one of the circuits, the parameter functions representing a relationship  
6 among design parameters of the subsystem, the design parameters including constraint and  
7 optimizing sets;

8           (b) a second code segment to select initial design points on the parameter functions  
9 having a first sum of the constraint set and a second sum of the optimizing set such that the first  
10 sum satisfies the design constraints; and

11          (c) a third code segment to select new design points on the parameter functions such  
12 that the second sum is improved within the design constraints.

1           12. (AMENDED) The machine readable medium of claim 11 wherein the first code  
2 segment comprises:

3           (a1) a code segment to configure each circuit of the plurality of circuits; and

4           (a2) a code segment to generate values of design parameters for each circuit according  
5 to the configured circuit, the values providing the parameter functions.

1           13. (AMENDED) The machine readable medium of claim 12 wherein the constraint  
2 set includes constraint parameters having values selectable to meet the design constraints and the  
3 optimizing set includes optimizing parameters having values to be optimized.

1           14. (AMENDED) The machine readable medium of claim 13 wherein the third code  
2 segment comprises:

3           (c1) a code segment to select values of the constraint parameters to meet the design  
4 constraints;

5           (c2) a code segment to determine values of the optimizing parameters corresponding  
6 to the selected values of the constraint parameters based on the parameter functions; and

7           (c3) a code segment to iterate (c1) and (c2) until values of the optimizing parameters  
8 are within a predetermined optimal range.

1           15. The machine readable medium of claim 13 wherein the constraint parameters  
2 include a delay parameter and the optimizing parameters include a power parameter.

1           16. The machine readable medium of claim 15 wherein the design constraints include  
2 a delay constraint.

1           17. (AMENDED) The machine readable medium of claim 16 wherein (a1) comprises:  
2 a code segment to size components in each circuit.

1           18. (AMENDED) The machine readable medium of claim 16 wherein (a1) comprises:  
2 a code segment to select a design technology for each circuit, the design technology  
3 being one of static and dynamic technologies.

1           19. (AMENDED) The machine readable medium of claim 18 wherein (a2) comprises:  
2 (a21) a code segment to generate a circuit netlist representing the configured circuit;  
3 (a22) a code segment to generate a timing file based on the circuit netlist using a circuit  
4 critical path;  
5 (a23) a code segment to determine power vectors of the configured circuit based on the  
6 circuit netlist;  
7 (a24) a code segment to calculate timing values; and  
8 (a25) a code segment to calculate power values.

1           20. (AMENDED) The machine readable medium of claim 19 wherein the third code  
2 segment comprises:

3           (c1) a code segment to select values of the delay parameter within the delay  
4 constraints;

5           (c2) a code segment to determine values of the power parameter corresponding to the  
6 selected values of the delay parameter based on the parameter function; and

7           (c3) a code segment to iterate (c1) and (c2) until values of the power parameter are  
8 within a predetermined optimal range.

1           22. (THREE TIMES AMENDED) A system comprising:

2           a memory for storing program instructions;

3           a processor coupled to the memory to execute the program instructions, the program  
4 instructions when executed by the processor interacting with tools provided by a design  
5 environment causing the processor to at least

6           (a) create parameter functions for a plurality of circuits in a subsystem, the subsystem  
7 having design constraints, each one of the parameter functions corresponding to each one of the  
8 circuits, the parameter functions representing a relationship among design parameters of the  
9 subsystem, the design parameters including constraint and optimizing sets,

10          (b) select initial design points on the parameter functions having a first sum of the  
11 constraint set and a second sum of the optimizing set such that the first sum satisfies the design  
12 constraints; and

13          (c) select new design points on the parameter functions such that the second sum is  
14 improved within the design constraints.

1           23. (AMENDED) The system of claim 22 wherein the program instructions causing  
2 the processor to create the parameter functions causes the processor to:

3           (a1) configure each circuit of the plurality of circuits; and

4           (a2) generate values of design parameters for each circuit according to the configured  
5 circuit, the values providing the parameter functions.

1           24. (AMENDED) The system of claim 22 wherein the constraint set includes  
2 constraint parameters having values selectable to meet the design constraints and the optimizing  
3 set includes optimizing parameters having values to be optimized.

1           25. (AMENDED) The system of claim 24 wherein the program instructions causing  
2 the processor to select the new design points causes the processor to:  
3           (c1) select values of the constraint parameters to meet the design constraints;  
4           (c2) determine values of the optimizing parameters corresponding to the selected values  
5 of the constraint parameters based on the parameter functions; and  
6           (c3) iterate (c1) and (c2) until values of the optimizing parameters are within a  
7 predetermined optimal range.

1           26. The system of claim 24 wherein the constraint parameters include a delay  
2 parameter and the optimizing parameters include a power parameter.

1           27. The system of claim 26 wherein the design constraints include a delay constraint.

1           28. (NEW) A method comprising:  
2           (a) generating first and second parameter functions for a circuit corresponding to first and  
3 second technologies, each of the first and second parameter functions relating a constraint  
4 parameter and an optimizing parameter;  
5           (b) selecting a first initial design point and a first new design point on the first parameter  
6 function such that the first new design point corresponds to a first improved optimizing  
7 parameter within a design constraint;  
8           (c) selecting a second initial design point and a second new design point on the second  
9 parameter function such that the second new design point corresponds to a second improved  
10 optimizing parameter within the design constraint; and  
11           (d) selecting the first technology if the first improved optimizing parameter is better than  
12 the second improved optimizing parameter, else selecting the second technology.

1           29. (NEW) The method of claim 28 wherein the first technology is a dynamic  
2 technology and the second technology is a static technology.

## REMARKS

Claims 1-20, and 22-27 are pending in the present application.

This Amendment is in response to the Office Action mailed April 24, 2001. In the Office Action, the Examiner objected to the title and abstract, provisionally rejected Claims 1-20 and 22-27 under 35 U.S.C. § 101 for double patenting, and rejected Claims 1-20 and 22-27 under 35 U.S.C. § 102. In response, Applicant has amended Claims 1, 3, 11, 13, 22, and 24 and add new claims 28 and 29. Applicant submits that the new claims 28 and 29 introduce no new matter. Support for new claims 28 and 29 is found in Figure 4 and Specification on page 17 (lines 6-24), page 18 (lines 1-5), and page 21 (lines 10-13). Reconsideration in light of the amendments and remarks made herein is respectfully requested.

### I. TITLE

In the Office Action, the examiner objected to the amended title. In particular, the Examiner stated that the title of the invention is not descriptive. In response, Applicant has amended the title to change to DESIGN OPTIMIZATION OF CIRCUITS BY SELECTING DESIGN POINTS ON PARAMETER FUNCTIONS TO IMPROVE OPTIMIZING PARAMETERS OF CIRCUITS WITHIN DESIGN CONSTRAINTS.

Therefore, Applicant respectfully requests the objection to the title be withdrawn.

### II. ABSTRACT

In the Office Action, the Examiner objected to the Abstract. In response, Applicant has amended the Abstract to recite the novelty of the invention. Therefore, Applicant requests the objection to the Abstract be withdrawn.

### **III. REJECTION UNDER 35 U.S.C. § 102(E)**

In the Office Action, the Examiner rejected Claims 1-20, and 22-27 under 1) 35 U.S.C. § 102(e) as anticipated by U.S. Patent No. 5,838,947 issued to Sarin ("Sarin") or U.S. Patent No. 5,880,967 issued to Jyu et al. ("Jyu"), 2) under § 102(a) as being anticipated by U.S. Patent No. 5,835,380 issued to Roething ("Roething") and 3) under § 102(b) as being anticipated by U.S. Patent No. 5,619,420 issued to Breid ("Breid"). Applicant respectfully traverses the rejections for the following reasons.

Applicant reiterates the arguments against the rejections as set forth in the previous response. In addition, Applicant submits that Sarin, Jyu, Roething and Breid, taken alone or in any combination, do not disclose, suggest, or render obvious selecting initial design points having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints; and (2) selecting new design points for the parameter functions such that the second sum is improved within the design constraints. These aspects of the invention are supported in the specification on page 19 (lines 6-11), page 20 (lines 19-24), and page 21 (lines 1-9) and is recited in amended Claims 1, 11, and 22 as follows:

“... initial design points on the parameter functions having a first sum of the constraint set and a second sum of the optimizing set such that the first sum satisfies the design constraints; and ... new design points on the parameter functions such that the second sum is improved within the design constraints.” (Amended Claims 1, 11, and 22)

Applicant has also amended Claims 3, 13, and 24 to correct minor informalities.

Therefore, Applicant believes that independent Claims 1, 11, and 22 and their respective dependent Claims are distinguishable over the cited prior art references. Accordingly, Applicant respectfully requests the rejections under 35 U.S.C. § 102(b) be withdrawn.

**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

**ABSTRACT**

Please delete the Abstract and insert the following in lieu thereof:

--One embodiment of the present invention is a method and machine readable medium for determining optimal values of design parameters of a subsystem to meet design constraints. The subsystem includes a number of circuits. A parameter function is created for the corresponding circuits. The parameter function represents a relationship among design parameters of the subsystem. The design parameters include constraint and optimizing sets. Initial design points for the parameter functions having a first sum of the constraint sets and a second sum of the optimizing sets are selected to such that the first sum satisfies the design constraints. New design points for the parameter functions are selected such that the second sum is improved while the first sum is within the design constraints.--

**CLAIMS**

- 1        1. (THREE TIMES AMENDED) A method comprising:
  - 2            (a) creating parameter functions for a plurality of circuits in a subsystem, the subsystem  
3            having design constraints, each one of the parameter functions corresponding to each one of the  
4            circuits, the parameter functions representing a relationship among [the] design parameters of the  
5            subsystem, the design parameters including constraint and optimizing sets;
  - 6            (b) selecting initial design points [for] on the parameter functions [to satisfy] having a  
7            first sum of the constraint set and a second sum of the optimizing set such that the first sum  
8            satisfies the design constraints; and
  - 9            (c) selecting new design points [for] on the parameter functions [to optimize design  
10          parameters] such that the second sum is improved within the design constraints.

- 1        3. (AMENDED) The method of claim 2 wherein [the design parameters include  
2            constraint and optimizing sets,] the constraint set [including] includes constraint parameters

3 having values selectable to meet the design constraints[,] and the optimizing set [including]  
4 includes optimizing parameters having values to be optimized.

1        11. (TWICE AMENDED) A machine readable medium having embodied thereon a  
2 computer program for processing by a machine, the computer program comprising:

3            (a) a first code segment to create parameter functions for a plurality of circuits in a  
4 subsystem, the subsystem having design constraints, each one of the parameter functions  
5 corresponding to each one of the circuits, the parameter functions representing a relationship  
6 among [the] design parameters of the subsystem, the design parameters including constraint and  
7 optimizing sets;

8            (b) a second code segment to select initial design points [for] on the parameter  
9 functions [to satisfy] having a first sum of the constraint set and a second sum of the optimizing  
10 set such that the first sum satisfies the design constraints; and

11            (c) a third code segment to select new design points [for] on the parameter functions  
12 [to optimize design parameters] such that the second sum is improved within the design  
13 constraints.

1        13. (AMENDED) The machine readable medium of claim 12 wherein [the design  
2 parameters include constraint and optimizing sets,] the constraint set [including] includes  
3 constraint parameters having values selectable to meet the design constraints[,] and the  
4 optimizing set [including] includes optimizing parameters having values to be optimized.

1        22. (THREE TIMES AMENDED) A system comprising:

2            a memory for storing program instructions;

3            a processor coupled to the memory to execute the program instructions, the program  
4 instructions when executed by the processor interacting with tools provided by a design  
5 environment causing the processor to at least

6            (a) create parameter functions for a plurality of circuits in a subsystem, the subsystem  
7 having design constraints, each one of the parameter functions corresponding to each one of the  
8 circuits, the parameter functions representing a relationship among [the] design parameters of the  
9 subsystem, the design parameters including constraint and optimizing sets,

10           (b) select initial design points [for] on the parameter functions [to satisfy] having a  
11 first sum of the constraint set and a second sum of the optimizing set such that the first sum  
12 satisfies the design constraints; and

13           (c) select new design points [for] on the parameter functions [to optimize design  
14 parameters] such that the second sum is improved within the design constraints.

1           24. (AMENDED) The system of claim 22 wherein [the design parameters include  
2 constraint and optimizing sets,] the constraint set [including] includes constraint parameters  
3 having values selectable to meet the design constraints[,] and the optimizing set [including]  
4 includes optimizing parameters having values to be optimized.

1           28. (NEW) A method comprising:

2           (a) generating first and second parameter functions for a circuit corresponding to first and  
3 second technologies, each of the first and second parameter functions relating a constraint  
4 parameter and an optimizing parameter;

5           (b) selecting a first initial design point and a first new design point on the first parameter  
6 function such that the first new design point corresponds to a first improved optimizing  
7 parameter within a design constraint;

8           (c) selecting a second initial design point and a second new design point on the second  
9 parameter function such that the second new design point corresponds to a second improved  
10 optimizing parameter within the design constraint; and

11           (d) selecting the first technology if the first improved optimizing parameter is better than  
12 the second improved optimizing parameter, else selecting the second technology.

1           29. (NEW) The method of claim 28 wherein the first technology is a dynamic  
2 technology and the second technology is a static technology.

## CONCLUSION

In view of the amendments and remarks made above, it is respectfully submitted that pending claims are in condition for allowance, and such action is respectfully solicited.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: October 24, 2001

  
THINH V. NGUYEN  
Reg. No. 42,034

### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on: October 24, 2001.

  
Barbara Hayashi

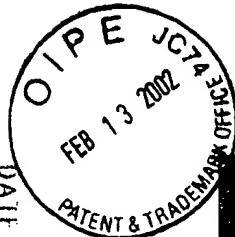
October 24, 2001  
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DESIGN OPTIMIZATION OF CIRCUITS BY SELECTING DESIGN POINTS  
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OF CIRCUITS WITHIN DESIGN CONSTRAINTS  
APP #09/148,392  
FILED 9/4/98  
INVENTOR BAEZ  
042390.P5512 TVN/BH  
12626